ABSTRACT

Methods and structures for an improved processor pipeline to eliminate the effect of correctible soft errors on processor/memory pipeline performance. Features and aspects hereof provide that the pipeline is extended by the addition of one or more information correction stages to correct a soft error using the fetched unit of information and the associated error correcting codes. By extending the pipeline, soft error correction does not stall the pipeline and hence system performance is improved in the face of soft errors from an error correcting memory subsystem.